ITE IT8785E Watchdog Timer Instructions

POST GUIDE

WDT and PWRGD share the same PIN.

1. **LDN7/23<4>=1**

8.3.6 Clock Selection Register (Index=23h, Default=00h)

Bit	Description
7-5	Reserved
4	Clock Source Select of Watch Dog Timer 0: Internal oscillating clock (Default) 1: External CLKIN

2. **LDN07/72<4>=1 ; enable WDT, LDN07/72 ; define WDT timer unit**

8.10.9 Watch Dog Timer Configuration Register (Index=72h, Default=001s0000b)

Bit	Description
7	**WDT Time-out Value Select 1** 1: Second 0: Minute
6	**WDT Output through KRST (pulse) Enable** 1: Enable 0: Disable
5	**WDT Time-out Value Extra Select** 1: 62.5ms x WDT Timer-out value (default = 3.5s) 0: Determined by WDT Time-out value select 1 (bit 7 of this register)
4	**WDT Output through PWRGD Enable** 1: Enable 0: Disable *During LRESET# this bit is selected by JP2 power-on strapping option.*
3-0	**Interrupt Level Select for WDT** Please refer to Table 8-13. Interrupt Level Mapping Table on page 82.

3. **LDN07/73/74 set value (start counting down after writing 73)**

8.10.10 Watch Dog Timer Time-out Value (LSB) Register (Index=73h, Default=38h)

Bit	Description
7-0	WDT Time-out Value 7-0

8.10.11 Watch Dog Timer Time-out Value (MSB) Register (Index=74h, Default=00h)

Bit	Description
7-0	WDT Time-out Value 15-8

If counter is 0, PWROK will have a low puse and status will be LDN07/71<0>

8.10.8 Watch Dog Timer Control Register (Index=71h, Default=00h)

Bit	Description
7	WDT is reset upon a CIR interrupt.
6	WDT is reset upon a KBC(Mouse) interrupt.
5	WDT is reset upon a KBC(Keyboard) interrupt.
4	**WDT Status will not be cleared by VCCOK or LRESET#, and only be cleared while write one to WDT Status** 1: Enable 0: Disable
3-2	**Reserved**
1	**Force Time-out** This bit is self-cleared.
0	**WDT Status** 1: WDT value is equal to 0. 0: WDT value is not is equal to 0.

WDT and PWROK have the same characteristics. Any of VIN2, AVCC (pin94), SUSB, ATXPG can be LOW. PWRGD is also LOW.

Figure 11-13. PWRGD1/2/3 Signal Condition

